

REMARKS

Claims 1-4, 12-13, 17-19, 24 are provisionally rejected under 35 U.S.C. 102(e) as being anticipated by copending Application No. 10/249,218. Claims 5-11, 14-16, 20-23 would be allowable if rewritten in independent form.

1. Correction of the specification:

There are some typo errors in paragraph [0026]. Therefore, the specification is corrected as shown in AMENDMENTS TO THE SPECIFICATION section. No new matter is entered. Acceptance of the corrected specification is therefore politely requested.

2. Correction of the claim:

A typo error occurs in claim 5, which is corrected as shown in AMENDMENTS TO THE CLAIM section. No new matter is entered. Acceptance of the corrected claim 5 is therefore politely requested.

3. Rejection of claims 1-4, 12-13, 17-19, 24 under 35 U.S.C. 102(e):

Claims 1-4, 12-13, 17-19, 24 are provisionally rejected under 35 U.S.C. 102(e) as being anticipated by copending Application No. 10/249,218 (publication 2004/0119072) which has a common assignee with the instant application. For reasons of record that can be found on pages 2-4 in the Office action identified above, which is part of paper no./mail date 20040709.

This provisional rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the copending application was derived from the inventor of this application and is thus not the invention "by another", or by an appropriate showing under 37 CFR 1.131. This rejection may not be overcome by the filing of a terminal disclaimer.

Response:

Although the copending Application No. 10/249,218 and the present application have a common assignee, they do not have any common inventors. Therefore, to
5 overcome this rejection, the Applicants will state the patentable differences between Lee et al. (Application No. 10/249,218) and the claims of this present application.

Claim 1 is amended to replace "forming a microcrystalline silicon layer" with
"depositing a microcrystalline silicon layer" as shown in the AMENDMENTS TO
10 THE CLAIMS section for describing the characteristics of the present application specifically, according to the specification of the present application (paragraph [0023]). The Applicants intend to point out the difference between the amended claim 1 of the present application and Lee et al. The amended claim 1 of the present application is repeated below:

15

"1. A method for forming a thin film transistor (TFT) of an organic light emitting display (OLED), the method comprising the steps of:
providing a substrate;
depositing a first metal layer on the substrate;
20 performing a first photo-etching-process (PEP) to remove a portion of the first metal layer to form a gate of the TFT on the surface of the substrate;
forming a gate insulating layer on the gate;
depositing a microcrystalline silicon layer on the gate insulation layer;
forming an amorphous silicon layer on the microcrystalline silicon layer;
25 forming a doped n+ layer on the amorphous silicon layer;
performing a second PEP to remove a portion of the doped n+ layer, the amorphous silicon layer, and the microcrystalline silicon layer;
forming a second metal layer on the substrate;
performing a third PEP to form a source and a drain of the TFT on the surface of
30 the substrate, and simultaneously to remove a portion of the doped n+ layer to expose the amorphous silicon layer; and
forming a passivation layer on the substrate."

Accordingly, one of the main characteristics of the present application is that *the microcrystalline silicon layer is deposited on the gate insulation layer by a PECVD process*. Then, the amorphous silicon layer and the doped n+ layer are sequentially
5 formed on the microcrystalline silicon layer. Furthermore, the gate insulating layer, microcrystalline silicon layer, and the amorphous silicon layer may be formed through a same PECVD process with continuous deposition (see paragraph [0027] and paragraph [0023] lines 5-8).

10 Lee et al. also teach forming a crystalline silicon layer on the gate insulating layer before forming an amorphous silicon layer and a doped n+ layer to prevent an increased threshold voltage. However, the method disclosed by Lee et al. for forming the crystalline silicon layer comprises forming a first amorphous silicon layer (46) on the gate insulating layer (44), performing a dehydrogen treatment to remove hydrogen
15 atoms in the first amorphous silicon layer (46), and performing a re-crystallizing process to transfer the first amorphous silicon layer (46) into a crystalline silicon layer (48). After that, a second amorphous silicon layer (50) and a doped n+ layer (52) are formed on the crystalline silicon layer (48) (see paragraph [0016]-[0017]).

20 Accordingly, according to Lee et al., the method for forming the crystalline silicon layer on the gate insulating layer is quite different from the method of the present application. This is because *Lee et al. teach first forming an amorphous silicon layer, and then treating and re-crystallizing the amorphous silicon layer to form a crystalline silicon layer*. In contrast to Lee et al., *the method of the present*
25 *application deposits a microcrystalline silicon layer on the gate insulating layer without any amorphous layers*. From the above discussion, the Applicants believe the method disclosed by Lee et al. is quite different from the method disclosed in the amended claim 1. Reconsideration of the amended claim 1 is hereby requested.

30 Since claims 2-4 and 12 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Reconsideration of claims 2-4 and 12 is therefore requested.

Regarding the other independent claim 13 of the present application, the Applicants also intend to point out the difference between Lee et al. and claim 13, which is repeated below:

5

“13. A method for forming a TFT of an OLED, the method comprising the steps of:
providing a substrate;
depositing a first metal layer on the substrate;
performing a first PEP to remove a portion of the first metal layer to form a gate
10 of the TFT on the surface of the substrate;
forming a gate insulating layer on the gate;
performing a surface treatment to the surface of the gate insulating layer;
forming a microcrystalline silicon layer on the gate insulating layer;
forming an amorphous silicon layer on the microcrystalline silicon layer;
15 forming a doped n+ layer on the amorphous silicon layer;
performing a second PEP to remove a portion of the doped n+ layer, the amorphous silicon layer, and the microcrystalline silicon layer;
forming a second metal layer on the substrate;
performing a third PEP to form a source and a drain of the TFT on the surface of
20 the substrate, and simultaneously to remove a portion of the doped n+ layer for exposing the amorphous silicon layer; and
forming a passivation layer on the substrate.”

Claim 13 discloses another main characteristic of the present application, in that
25 *a surface treatment to the surface of the gate insulating layer is performed after forming the gate insulating layer and before forming the microcrystalline silicon layer. The main function of the surface treatment to the gate insulating layer is to make the gate insulating layer have stronger oxygen bonding with the subsequently formed microcrystalline silicon layer so as to produce a stable interface between the gate*
30 *insulating layer and the microcrystalline silicon layer (paragraph [0026]).*

The Examiner alleges that Lee et al. also teach performing a surface treatment on

the gate insulating layer. However, according to the disclosure of Lee et al., *the target of the dehydration treatment and re-crystallizing process is the first amorphous silicon layer, not the gate insulating layer, for forming the crystalline silicon layer* (paragraph [0017]). Consequently, *the surface treatment process according to Lee et al.*
5 *does not have the function to produce stronger oxygen bonding between the gate insulating layer and the crystalline silicon layer.* Therefore, both the target and function of the surface treatment of the method according Lee et al. is quite different from the method according to claim 13 of the present application. In view of the above discussion, the Applicants politely request the Examiner to reconsider the rejection of
10 claim 13.

Claims 17-19 and 24 are dependent upon claim 13. Therefore, claims 17-19 and 24 should be allowed if claim 13 is allowed. Reconsideration of claims 17-19 and 24 is hereby requested.

15

4. Double patenting:

Claims 1-4, 12-13, 17-19, 24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being anticipated over claims 1-16 of copending Application No. 10/249,218. For reasons of record that can be
20 found on pages 4-5 in the Office action identified above, which is part of paper no./mail date 20040709.

Response:

Since the differences between the amended claim 1 and claim 13 of the present
25 application and Lee et al. have been stated in the above description, the Applicants believe the rejection of double patenting is successfully traversed.

5. Allowable subject matter:

Claims 5-11, 14-16, 20-23 objected to as being dependent upon a rejected base
30 claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

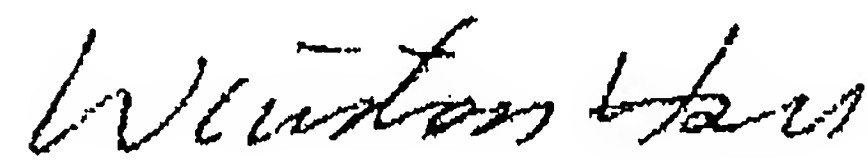
Response:

As claims 5-11 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. As claims 14-16 and 20-23 are dependent upon claim 13, they should be allowed if claim 13 is allowed.

5

Sincerely yours,

10



Date: October 8, 2004

Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506

Merrifield, VA 22116

15

U.S.A.

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

(Please contact me by e-mail if you need a telephone communication and I will return your call promptly.)

20